

Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No. BDG005		Serial No. 10/042,812	
<b>INFORMATION DISCLOSURE STATEMENT</b> (Use several sheets if necessary)				Applicant Cheng-Lien Chiang			
				Filing Date January 9, 2002		Group Art Unit	
<b>U.S. Patent Documents</b>							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
C.C.	AA	5,081,520	01/1992	Yoshii et al.	357	80	
C.C.	AB	5,241,133	08/1993	Mullen, III et al.	174	52.4	
C.C.	AC	5,394,303	02/28/95	Yamaji	361	749	
C.C.	AD	5,665,652	09/1997	Shimizu	438	127	
C.C.	AE	5,674,785	10/1997	Akram et al.	437	217	
C.C.	AF	5,744,827	04/28/98	Jeong et al.	257	686	
C.C.	AG	5,744,859	04/1998	Ouchida	257	668	
C.C.	AH	5,804,771	09/1998	McMahon et al.	174	255	
C.C.	AI	5,811,879	09/1998	Akram	257	723	
C.C.	AJ	5,949,655	09/1999	Glenn	361	783	
C.C.	AK	6,013,877	01/2000	Degani et al.	174	264	
C.C.	AL	6,143,588	11/2000	Glenn	438	116	
C.C.	AM	6,159,770	12/2000	Tetaka et al.	438	112	
C.C.	AN	6,274,927	08/2001	Glenn	257	680	
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
C.C.	AO	Crowley, "Socket Developments for CSP and FBGA Packages," Chip Scale Review, May 1998, pp. 37-40.					
C.C.	AP	Forster, "Socket Challenges for Chip-Scale Packages," Chip Scale Review, May 1998, pp. 43-47.					
C.C.	AQ	Amagai, "Chip-Scale Packages for Center-Pad Memory Devices," Chip Scale Review, May 1998, pp. 68-77.					
C.C.	AR	Vandeveld et al., "The PSGA, a Lead-Free CSP for High Performance & High Reliable Packaging," Proceedings of the 2001 International Symposium on Microelectronics, October 9, 2001, pp. 260-265.					
Examiner <i>Christina</i>		Date Considered 4/17/03					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.							



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C.C.	AA	U.S. Application Serial No. 09/865,367, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"	
C.C.	AB	U.S. Application Serial No. 09/864,555, filed May 24, 2001, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"	
C.C.	AC	U.S. Application Serial No. 09/864,773, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"	
C.C.	AD	U.S. Application Serial No. 09/878,649 filed June 11, 2001, entitled "Method of Making a Semiconductor Chip Assembly with a Conductive Trace Subtractively Formed Before and After Chip Attachment"	
C.C.	AE	U.S. Application Serial No. 09/878,626 filed June 11, 2001, entitled "Method of Connecting a Conductive Trace to a Semiconductor Chip"	
C.C.	AF	U.S. Application Serial No. 09/917,339 filed July 27, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace to a Semiconductor Chip"	
C.C.	AG	U.S. Application Serial No. 09/927,216 filed August 10, 2001, entitled "Semiconductor Chip Assembly with Hardened Connection Joint"	
C.C.	AH	U.S. Application Serial No. 09/939,140 filed August 24, 2001, entitled "Semiconductor Chip Assembly with Interlocked Conductive Trace"	
C.C.	AI	U.S. Application Serial No. 09/962,754 filed September 24, 2001, entitled "Method of Connecting a Conductive Trace and an Insulative Base to a Semiconductor Chip"	
C.C.	AJ	U.S. Application Serial No. 09/972,796 filed October 6, 2001, entitled "Method of Connecting a Bumped Compliant Conductive Trace and an Insulative Base to a Semiconductor Chip"	
C.C.	AK	U.S. Application Serial No. 09/997,973 filed November 29, 2001, entitled "Method of Connecting a Bumped Conductive Trace to a Semiconductor Chip"	
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